

IBM POUGHKEEPSIE

Diagnostic Engineering Publication

1410/7010

Dept. B59, Bldg. 965
Date 11/15/63

Subject: Diagnostic Program CC01A - 1410/7010 Limited CPU
Sequence Number 001 Instruction Test
Replaces New Program

This Program uses no System or Channel Control Cards

This Program should be run only from tape.

Enclosures: 44 Pages
Card Deck for CARD ONLY SYSTEMS (as punched by UP51)
8 Cards - Card Loader (1-7) and 1 Core Clear
160 Cards No. 001-160 Data Cards
1 Card Execute Card

Distribution: X 1410
X 7010
Other

CC01A
Page 001

CC01A

11/15/1963

1410/7010 LIMITED CPU INSTRUCTION TEST

CONTENTS OF CC01 WRITE UP AND LISTING

2.xx.00.0	Test Description	Page 003
2.xx.01.0	Loading Procedures	Page 004
2.xx.02.0	Operating Procedures	Page 004
2.xx.03.0	Operating Hints and Comments	Page 004
2.xx.04.0	Program Stops and Restarts	Page 005
2.xx.05.0	Typeouts	Page 005
2.xx.06.0	Flow Charts	Page 006
2.xx.07.0	Appendix	Page N/A
2.xx.08.0	Listing	Page 001
	Summary	Page 038

2.xx.00.0 TEST DESCRIPTION

2.xx.00.1 MODIFICATIONS

CC01A is the first release version of this program and it does not obselete any program.

2.xx.00.2 DESCRIPTION

CC01 was taken directly from C021 to test enough of the basic instruction set to read in and operate the Tape Control Program. It does not contain any Error Typeouts, Loops, Tad Controls or Options to repeat, it is strictly a special purpose test that runs prior to the Tape Control Program and halts for any error.

The Load Program utilizes a few instructions to Load CC01 and they are: BCE, MRCW, MLCS, BA1, RT, BEX1 , MLCWA and a Branch instruction.

This test will only be used in conjunction with the Tape Control Program operating from tape.

2.xx.00.3 EQUIPMENT REQUIRED

Minimum Storage
One tape Unit on any channel
Console Printer

2.xx.00.4 CARD DECK

7	Cards	L1 Loader
1	Card	Core Clear
160	Cards	Program Cards
1	Card	Execute (Branch to 1972) to operate TC50

2.xx.00.5 ENGINEERING LEVEL

CC01 will operate on any 1410/7010 system unless an Engineering Change modifies the operations of the standard Instruction set.

2.xx.01.0 LOADING PROCEDURES

2.xx.01.1 1410 TAPE INPUT

A. Display and Alter Locations 00000-00011 as follows:

v v v
1. RL?B000011\$. If tape unit on E channel
v v v
2. XL?B000011\$. If tape unit on F channel

B. Set Mode switch to RUN, Computer Reset and Start.

2.xx.01.2 7010 TAPE INPUT

A. If tape unit is on E channel, use 7010 Load Key and disregard steps (B) and (C)

B. If tape unit is not on E channel, Display and Alter Locations 00000-00011 as follows:

v v v
1. XL?B000011\$. If tape unit on F channel
v v v
2. 3L?B000011\$. If tape unit on G channel
vv v
3. 1L!B000011\$. If tape unit on H channel

C. Set MODE switch to Run, Computer Reset and Start.

2.xx.02.0 OPERATING PROCEDURES

No special instructions are necessary to run this program. The test is ONE, QUICK check of a portion of the basic instruction set and unless there is an error it immediately reads in TC50 and begins to operate TC50

2.xx.03.0 OPERATING HINTS AND COMMENTS

If there is an error the program will stop. The CE must then consult the listing to find out which instruction failed and determine if he can continue. It is possible to continue to the next instruction by pushing the Start Key. If a number of errors occur it would not be possible for TC50 to operate. If there are a few errors it may be possible that TC50 will work and be able to bring into Core C020 or C021 to completely check out CPU instructions and give the CE the benefit of different Loops and Options.

At Location 01000-01100 is a pattern of characters to be looked at only by the C.E to determine if there are any Information Transfer errors between TAU and CPU.

2.xx.04.0 PROGRAM STOPS

All stops are Error Stops

2.xx.05.0 TYPEOUTS

2.xx.05.1 NORMAL

"CC01A" Test Ident.

"CC01 COMPLETE" Indicate End of Test.

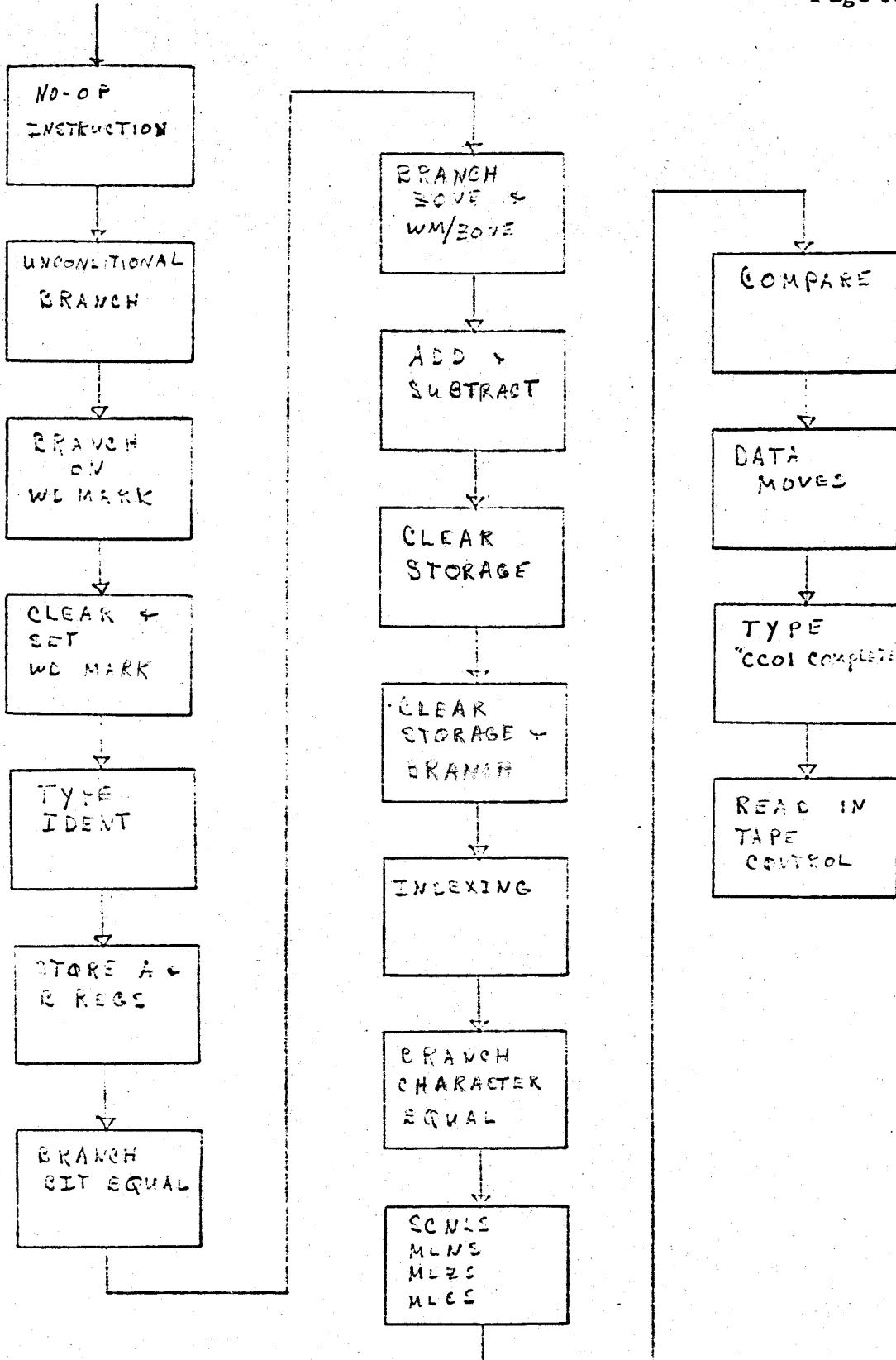
2.xx.05.2 ERROR

None.

2.00000

FLOW CHART

CC01
Page 006



CC01 PAGE 1
CPU TEST
OPCOD OPERAND
CT ADDRS INSTRUCTION

PGLIN	LABEL	CIL	OPCOD	OPERAND	CIL	OPCOD	OPERAND	CT	ADDRS	INSTRUCTION
10C2		2			2					
10C3		LOAD			LOAD					
1004	CTLIND	EQU	1245		EQU	1245				
1005	IDENT	EQU	1250		EQU	1250				
10C6	START	EQU	2000		EQU	2000				
10C7	*									
10C8		ORG	CTLIND		ORG	CTLIND				
1009		DC	00010R3		DC	00010R3	SEQUENCE AND MEM SIZE	5	01249	
1010	*									
1011	*	ORG	IDENT		ORG	IDENT				
1012	*									
1013		DCW	ACCOLIAA.G		DCW	ACCOLIAA.G	PROGRAM IDENT	5	01254	
1014	*									
1015	*	ORG	1000		ORG	1000				
1016	*									
1017		DCW	311223344556677889900AABCCCCDDDEEEFGGA		DCW	311223344556677889900AABCCCCDDDEEEFGGA		34	01033	
1018			HHHIIJJKKLLMMNNNOOPPQQRRSSTTUUUVVWWXXaa			HHHIIJJKKLLMMNNNOOPPQQRRSSTTUUUVVWWXXaa		34	01067	
1019			LLGGRR.D.WBS.GTQ			LLGGRR.D.WBS.GTQ		32	01099	
1020	*									
1021	*	ORG	1800		ORG	1800				
1022	*									
1023		SBR	*69		SBR	*69	COMMON TYPE ROUTINE	7	01800	6 01815 B
1024		WCP	0		WCP	0		10	01807	M Z10 00000 W
1025		SBR	*E20		SBR	*E20		7	01817	G 01843 B
1026		BCBL	*-23		BCBL	*-23		7	01824	R 01807 2
1027		BAL	*E1		BAL	*E1		7	01831	R 01838 G
1028		B	0		B	0		7	01838	J 00000
1029	*									
1030	*									
1031		SBR	*661		SBR	*661	INTERNAL ADDRESS ALTER ROUTINE	7	01845	G 01912 B
1032		RCP	*E26		RCP	*E26		10	01852	M Z10 01887 R
1033		BEX1	*-16,M		BEX1	*-16,M		7	01862	R 01852 M
1034		BNT1	*E32		BNT1	*E32		7	01869	R 01907 S
1035		BAL	*E1		BAL	*E1		7	01876	R 01883 M
1036		RCPW	0		RCPW	0		10	01883	L Z10 00000 R

CPU TEST
OPCODE OPERAND

PGIN LABEL INSTRUCTION

1037 BEX1 *-16,S
1038 BAI *E1
1039 B 0

1040

1041 ORG START PROGRAM BEGINS HERE

02000

1042
1043 * ROUTINE 01.00 CHECK LONG NO-OP INSTRUCTION1044
1045 NOP 1 02000 N
1046 DC * 1234567890#*TTS/WBS/STUVWXYZ*,*SSSMa
1047 DC * R*D,LIGa
1048 DC * J-KLMNOPQR*\$*B,L&ABCDEFIGHIM,OBIGa
1049 *****1050 * ROUTINE 02.00 CHECK UNCOND BR INST. THIS ROUTINE ASSUMES THAT
1051 MM-HL WILL GIVE INSTRUCTION CK IF BRANCH FAILS1052 *
1053 *
1054 B *E1 SET AND STEP IAR TO SAME ADDRESS
1055 S *62 SHOULD SKIP FOLWNG INVALID OPCODE
1056 DCW a a 1 02079
1057 *****1058 *
1059 * ROUTINE 03.00 CHECK BRANCH ON WORD MARK INSTRUCTION
1060 AC BW AD,AD SHOULD NOT BR, INST CK IF IT DOES
1061 AC BW AE,*E1 SHOULD BRANCH, INST CK IF NO BR
1062 DCW a a 1 02104
1063 AD DC, aMa 1 02105
1064 *****

1065 * ROUTINE 04.00 CHECK CLEAR AND SET WORD MARK INSTRUCTIONS

1066 AE CW AC,AE TRY TO CLEAR WMS AT TWO PLACES
1067 AF BW AF-1,AC SHOULD NOT BR, INST CK IF IT DOES
1068 AE BW AF,AE DITTO
1069 SW AE,AC RESTORE WMS PREVIOUSLY CLEARED
1070 SW *E4,AE TEST AE FOR WORD MARK
1071 SW *****
1072 SW *****

PGLIN	LABEL	CC01 CPU TEST		CT ADDRS	INSTRUCTION	CC01 PAGE 3
		OPCODE	OPERAND			
1073	AF	DCW	a 12@ *E2,AC		INSTRUCTION CK IF NO WM AT AE TEST AC FOR WORD MARK	3 02166 12 02167 V 02180 02080 1
1074		DCW	a @		INSTRUCTION CK IF NO WM AT AC	1 02179
1075						
1076						
1077	*	ROUTINE 05.00	TYPE IDENT, CK TYPEWR BUSY, HALT, HALT/BR.			
1078	*	ROUTINE 05.00	TYPE IDENT, CK TYPEWR BUSY, HALT, HALT/BR.			
1079	*		THESE OPS PERFORMED ONLY FIRST TIME THROUGH			
1080	*					
1081		NOPWM			THIS BR NOT TAKEN FIRST TIME THRU	7 02181 J 02226
1082		B	AJ			6 02188 * 02181
1083		SW	*-12			10 02194 M ZTO 01250 W
1084	AG	WCP	IDENT			
1085		BCB1	*-16			7 02204 R 02194 2
1086		BA1	*E1			7 02211 R 02218 G
1087		ORG	*			7 02218
1088	AH	NOP				1 02218 N
1089		B	AJ			7 02219 J 02226
1090		ORG	*			02226
1091						
1092	*	ROUTINE 06.00	CHECK OPERATION OF SAR AND SBR INSTRUCTIONS			
1093	*					
1094	*					
1095	AJ	B	AK		I-ADDR MODIFIED WITHIN ROUTINE	7 02226 J 02233
1096	AK	NOPWM			NOTE. BR TO 00000 INDICATES SBR FAILURE	1 02233 N
1097		B	AL		BR TO 00001 INDICATES SAR FAILURE	7 02234 J 02286
1098		SW	AKE1			6 02241 * 02234
1099		CW	1,ANE1		SET UP A & B ADDR REGISTERS	11 02247 □ 00001 02288
1100		SBR	AJ65			7 02258 G 02231 B
1101		SAR	AJ65			7 02265 G 02231 A
1102		SBR	AJ65			7 02272 G 02231 B
1103		R	AJ			7 02279 J 02226
1104	AL	H				1 02286 *
1105	AN	CW	A0E1,2		SET UP A & B ADDR REGISTERS	11 02287 □ 02327 00002
1106		SAR	AJ65			7 02298 G 02231 A
1107		SBR	AJ65			7 02305 G 02231 B
1108		SAR	AJ65			7 02312 G 02231 A

PGLIN	LABEL	CPU TEST OPCODE	OPERAND	CC01 CT	ADDRS	INSTRUCTION
1109		B AJ		7	02319	J 02226
1110	A0	CW AK&1		6	02326	D 02234
1111		SAR AJ&5		7	02332	G 02231 A
1112		SH 1		6	02339	, 00001
1113	*****	*****	*****			
1114	*	ROUTINE 07.00	CHECK OPERATION OF BRANCH BIT EQUAL INSTRUCTION			
1115	*	ROUTINE 07.00	ROUTINE 07.00			
1116	*	ROUTINE 07.00	ROUTINE 07.00			
1117	*	SUB-RTN 07.01	BBE AP,*,1		12 02345	W 02358 02356 1
1118			H	1	02357	.
1119						
1120	*	SUB-RTN 07.02	BBE *E8,AQ&11,1		12 02358	W 02377 02389 1
1121			H			
1122	AP	BBE *E8,AQ&11,1	SHOULD NOT BRANCH		7	02370 J 02378
1123		B AQ			1	02377 .
1124		H				
1125	*	SUB-RTN 07.03	BBE *E8,AP&11,1		12 02378	W 02397 02369 1
1126	AQ	BBE *E8,AP&11,1	SHOULD NOT BRANCH		7	02390 J 02398
1127		B AR			1	02397 .
1128		H				
1129	*	SUB-RTN 07.04	BBE AU,*,2		12 02398	W 02411 02409 2
1130	AR	BBE AU,*,2	SHOULD BRANCH		1	02410 .
1131		H				
1132	*	SUB-RTN 07.05	BBE *E8,AX&11,2		12 02411	W 02430 02442 2
1133	AU	BBE *E8,AX&11,2	SHOULD NOT BRANCH		7	02423 J 02431
1134		B AX			1	02430 .
1135	AW	H				
1136	*	SUB-RTN 07.06	BBE *E8,AUC11,8		12 02431	W 02450 02422 8
1137	AX	BBE *E8,AUC11,8	SHOULD NOT BRANCH		7	02443 J 02451
1138		B BA			1	02450 .
1139	AZ	H				
1140	*	SUB-RTN 07.07	BBE BD,*,4		12 02451	W 02464 02462 4
1141	BA	BBE BD,*,4	SHOULD BRANCH		1	02463 .
1142	BC	H				
1143	*	SUB-RTN 07.08	BBE *E8,BGC11,4		12 02464	W 02483 02495 4
1144	BD	BBE *E8,BGC11,4	SHOULD NOT BRANCH			

PC/LIN	LABEL	CPU TEST		CT	ADDRS	PAGE	INSTRUCTION
		OPCODE	OPERAND				
1145		B	BG			7	02476 J 02484
1146	BF	H				1	02483 -
1147	* SUB-RTN 07.09		*E8,B0E11..				SHOULD NOT BRANCH
1148	BG	B8E	*E8,B0E11..			12	02484 W 02503 02475 .
1149		B	BJ			7	02496 J 02504
1150	BI	H				1	02503 -
1151	* SUB-RTN 07.10						SHOULD BRANCH
1152	BJ	B8E	BM,*+B			12	02504 W 02517 02515 8
1153	BL	H				1	02516 -
1154	* SUB-RTN 07.11						SHOULD BRANCH
1155	BM	B8E	*E8,B0E11..			12	02517 W 02536 02548 8
1156		B	BP			7	02529 J 02537
1157	BO	H				1	02536 -
1158	* SUB-RTN 07.12						SHOULD NOT BRANCH
1159	BP	B8E	*E8,B0E11..G			12	02537 W 02556 02528 G
1160		B	BS			7	02549 J 02557
1161	BR	H				1	02556 -
1162	* SUB-RTN 07.13						SHOULD BRANCH
1163	BS	B8E	BV,*+*			12	02557 W 02570 02568 +
1164	BU	H				1	02569 -
1165	* SUB-RTN 07.14						SHOULD NOT BRANCH
1166	BV	B8E	*E8,B0E11..\$			12	02570 W 02589 02601 \$
1167		B	BY			7	02582 J 02590
1168	BX	H				1	02589 -
1169	* SUB-RTN 07.15						SHOULD NOT BRANCH
1170	BY	B8E	*E8,B0E11..C			12	02590 W 02609 02581 C
1171		B	CB			7	02602 J 02610
1172	CA	H				1	02609 -
1173	* SUB-RTN 07.16						SHOULD BRANCH
1174	CB	B8E	CE,*,-			12	02610 W 02623 02621 -
1175	CD	H				1	02622 -
1176	* SUB-RTN 07.17						SHOULD NOT BRANCH
1177	CE	B8E	*E8,C0E11..-			12	02623 W 02642 02654 -
1178		B	CH			7	02635 J 02643
1179	CG	H				1	02642 -
1180	* SUB-RTN 07.18						

PGLIN	LABEL	CPU TEST OPCODE OPERAND	CT	ADDRS	INSTRUCTION
1181	CH	BDE *E8,C6E11,S	12	02643 W	02662 02634 S
1182		B CK	7	02655 J	02663
1183	CJ	H	1	02662 .	
1184	* SUB-RTN 07.19				
1185	CK	BDE *E8,..*	12	02663 W	02682 02674
1186		B CN	7	02675 J	02683
1187	CM	H	1	02682 .	
1188	* SUB-RTN 07.20				
1189	CN	BDE *E8,CQC11,	12	02683 W	02702 02714
1190		B CQ	7	02695 J	02703
1191	CP	H	1	02702 .	
1192	* SUB-RTN 07.21				
1193	CQ	BDE *E8,CNC11,P	12	02703 W	02722 02694 G
1194		B CA	7	02715 J	02723
1195	CS	H	1	02722 .	
1196	*****	*****			
1197	*				
1198	* ROUTINE 08.00	CHECK OPERATION OF BRANCH ZONE & BRANCH W/ZONE			
1199	*				
1200	* SUB-RTN 08.01				
1201	CA	BZN DD,TPMK.	12	02723 V	02736 09017 2
1202	CC	H	1	02735 .	
1203	* SUB-RTN 08.02				
1204	CD	BZN *E8,QUOT.	12	02736 V	02755 09032 2
1205		R DG	7	02748 J	02756
1206	CF	H	1	02755 .	
1207	* SUB-RTN 08.03				
1208	CG	BZN *E8,DELT.	12	02756 V	02775 09048 2
1209		B CJ	7	02768 J	02776
1210	CI	H	1	02775 .	
1211	* SUB-RTN 08.04				
1212	CJ	BZN *E8,GPMK.	12	02776 V	02795 09064 2
1213		B DM	7	02788 J	02796
1214	CL	H	1	02795 .	
1215	* SUB-RTN 08.05				
1216	DM	BZN DP,QUOT,*	12	02796 V	02809 09032 S

PGLIN	LABEL	C001 OPCOD	CPU TEST OPERAND	CC01 OPCOD	CPU TEST OPERAND	CT ADDRS	PAGE INSTRUCTION
1217	CO	H				1 02808	.
1218	* SUB-RTN 08.06						
1219	CP	BZN *E8,TPMK,*	DS		SHOULD NOT BRANCH	12 02809 V 02828 09017 S	
1220		B	DS			7 02821 J 02829	
1221	CR	H				1 02828	.
1222	* SUB-RTN 08.07						
1223	DS	BZN *E8,DELT,*	DV		SHOULD NOT BRANCH	12 02829 V 02848 09048 S	
1224		B	DV			7 02841 J 02849	
1225	DU	H				1 02848	.
1226	* SUB-RTN 08.08						
1227	DV	BZN *E8,GPMK,*	DY		SHOULD NOT BRANCH	12 02849 V 02868 09064 S	
1228		B	DY			7 02861 J 02869	
1229	CX	H				1 02868	.
1230	* SUB-RTN 08.09						
1231	CY	BZN EB,DELT,-		SHOULD BRANCH		12 02869 V 02882 09048 K	
1232	EA	H				1 02881	.
1233	* SUB-RTN 08.10						
1234	EB	BZN *E8,TPMK,-	EE		SHOULD NOT BRANCH	12 02882 V 02901 09017 K	
1235		B	EE			7 02894 J 02902	
1236	ED	H				1 02901	.
1237	* SUB-RTN 08.11						
1238	EE	BZN *E8,QUOT,-		SHOULD NOT BRANCH		12 02902 V 02921 09032 K	
1239		B EH				7 02914 J 02922	
1240	EG	H				1 02921	.
1241	* SUB-RTN 08.12						
1242	EH	BZN *E8,GPMK,-	EK	SHOULD NOT BRANCH		12 02922 V 02941 09064 K	
1243		B EK				7 02934 J 02942	
1244	EJ	H				1 02941	.
1245	* SUB-RTN 08.13						
1246	EK	BZN EN,GPMK,&		SHOULD BRANCH		12 02942 V 02955 09064 B	
1247	EM	H				1 02954	.
1248	* SUB-RTN 08.14						
1249	EN	BZN *E8,TPMK,&	EQ	SHOULD NOT BRANCH		12 02955 V 02974 09017 S	
1250		B EQ				7 02967 J 02975	
1251	EP	H				1 02974	.

PGLIN	LABEL	OPCODE	OPERAND	COMMENT	PC	OPCODE	OPERAND	COMMENT	PC
1252	* SUB-RTN 08.15			SHOULD NOT BRANCH	12	02975	V 02994 09032 8		
1253	EQ	BZN	*E8,QUOT,E		7	02987	J 02995		
1254		H	ET		1	02994	*		
1255	ES	H							
1256	* SUB-RTN 08.16			SHOULD NOT BRANCH	12	02995	V 03014 09048 B		
1257	ET	BZN	*E8,DELT,E		7	03007	J 03015		
1258		B	EW		1	03014	*		
1259	EV	H							
1260	* SUB-RTN 08.17			SHOULD NOT BRANCH	12	03015	V 03034 09064 3		
1261	EW	BWZ	*E8,GPMK,		7	03027	J 03035		
1262		B	EZ		1	03034	*		
1263	EY	H							
1264	* SUB-RTN 08.18			OPCODE SHOULD	1	03035	V		
1265	EZ	BWZ		1-ADDRESS NOT	5	03040	03054		
1266		DC	FB	B-ADDRESS BRANCH	5	03045	09071		
1267			GMM	D-MODIFIER	1	03046			
1268			ABE	SHOULD BRANCH	7	03047	J 03055		
1269		B	*E2		1	03054	*		
1270	FB	H							
1271	*								
1272	* SUB-RTN 10.12			LONG ADD & SUBTRACT USING ALL DIGITS					
1273	HO	ZS	654321,WORK4-5	WORK4 SHOULD BE 5432J..... NOW	11	03055	* 09542 09166		
1274		ZS	WORK4-5,WORK4	WORK4 SHOULD BE 000005432A NOW	11	03066	* 09166 09171		
1275		A	E9876,WORK4-5	WORK4 SHOULD BE 098765432A NOW	11	03077	A 09546 09166		
1276		A	E123,WORK4-5	WORK4 SHOULD BE 099995432A NOW	11	03088	A 09549 09166		
1277		A	E45679,WORK4	WORK4 SHOULD BE 1000000006 NOW	11	03099	A 09554 09171		
1278		BZ	HP	SHOULD NOT BRANCH	7	03110	J 03219 V		
1279		SW	WORK4-B		6	03117	* 09163		
1280		ZS	WORK4		6	03123	*	09171	
1281		CW	WDRK4-B		6	03129	□ 09163		
1282		BZ	*E8	SHOULD BRANCH	7	03135	J 03149 V		
1283		B	HP		7	03142	J 03219		
1284		S	E123,WORK4-5	WORK4 SHOULD BE 098770000- NOW	11	03149	S 09549 09166		
1285		S	-45679,WORK4	WORK4 SHOULD BE 098765432J NOW	11	03160	S 09559 09171		
1286		S	E9876,WORK4-5	WORK4 SHOULD BE 000005432J NOW	11	03171	S 09546 09166		

PGLIN	LABEL	COD	CPU TEST OPCODE	OPERAND	CC01	CC01	CPU TEST PAGE	9
						CT	ADDRS	INSTRUCTION
1287		S	-54321,WORK4	WORK4 SHOULD BE 00000000- NOW SHOULD BRANCH	11	03182	S 09564	09171
1288	BZ	B	*E8		7	03193	J 03207	V
1289	B	H			7	03200	J 03219	
1290	BZN	HQ,WORK4,-		WILL BRANCH IF ZONED CORRECTLY	12	03207	V 03220	09171 K
1291	H				1	03219	.	
1292	*	SUB-RTN	10.13	CK B-FIELD ZONE RETENTION & SIGN CHANGE				
1293	HQ	SW	WORK5	PROTECT HI-ORDER FIELD OF WORKS	6	03220	S 09175	
1294	ZA	2A	-1,WORKS	INSURE ZONED NEGATIVELY	11	03226	H 09565	09175
1295	CW	WORK5		REMOVE WM	6	03237	U 09175	
1296	S	WORK5	*E8,WORKS,-	ZERO OUT WORKS FIELD	6	03243	S 09175	
1297	BZN	HR		* INSURE	12	03249	V 03268	09175 K
1298	B	HR		* THAT	7	03261	J 03435	
1299	BZN	*E8,WORKS-1,4		* ZONES	12	03268	V 03287	09174 S
1300	B	HR		* ARE	7	03280	J 03435	
1301	BZN	*E8,WORKS-2,		* RETAINED	12	03287	V 03306	09173 2
1302	B	HR		* FOLLOWING	7	03299	J 03435	
1303	BZN	*E8,WORKS-3,6		* SINGLE-FIELD	12	03306	V 03325	09172 B
1304	B	HR		* SUBTRACT	7	03318	J 03435	
1305	A	291YY@,WORKS			11	03325	A 09569	09175
1306	BZN	*E8,WORKS,6		* CHECK	12	03336	V 03355	09175 B
1307	B	HR		* SIGN	7	03348	J 03435	
1308	BZN	*E8,WORKS-1,4		* CHANGE	12	03355	V 03374	09174 S
1309	B	HR		* AND	7	03367	J 03435	
1310	BZN	*E8,WORKS-2,		* ZONE	12	03374	V 03393	09173 2
1311	B	HR		* RETENTION	7	03386	J 03435	
1312	BZN	*E8,WORKS-3,6		* FOLLOWING	12	03393	V 03412	09172 B
1313	B	HR		* ADD	7	03405	J 03435	
1314	S	FIVE9S-1,WORK5		SHOULD CHANGE SIGN BACK TO MINUS	11	03412	S 09252	09175
1315	BZN	*E2,WORKS,-		SHOULD BRANCH	12	03423	V 03436	09175 K
1316	HR	H			1	03435	.	
1317	*****	*****	*****	*****	*****	*****	*****	*****
1318	*	ROUTINE	11.00	CHECK OPERATION CLEAR STORAGE				
1319	*	ROUTINE						
1320	*	SUB-RTN	11.01	CK CS 0000C FOR NO ERR & PROPER SETTINGS AAR, BAR				
1321	*	ROUTINE						

PGLIN LABEL CPU TEST
OPCODE OPERAND

PGLIN	LABEL	CPU TEST	OPCODE	OPERAND	CT	ADDRS	INSTRUCTION
1322	HW	CS 0			6	03436 / 00000	
1323		SBR	MOLD81-1		7	03442 G 09185 B	
1324		SAR	MOLDAI		7	03449 G 09181 A	
1325		A 60,MOLDAI	CHECK SETTING OF AAR		11	03456 A 09570 09181	
1326		BZ *E8	SHOULD BRANCH		7	03467 J 03481 V	
1327		HX B			7	03474 J 03499	
1328		S FIVE9S,MOLD81-1	CHECK SETTING BAR		11	03481 S 09253 09185	
1329		BZ HY	SHOULD BRANCH		7	03492 J 03500 V	
1330	HX	H			1	03499 *	
1331	*	SUB-RTN 11.02	CHECK PROPER OPERATION CLEAR STORAGE				
1332	HY	SW HZ69	INITIALIZE B-FIELD		6	03500 * 03671	
1333		S HZ610	OF BBE INSTRUCTION		6	03506 S 03672	
1334		A FIVE9S-3,HZ610	WHICH FOLLOWS		11	03512 A 09250 03672	
1335		CW HZ69			6	03523 D 03671	
1336		SW 201,251			11	03529 * 00201 00251	
1337		CS 299	TRY TO CLEAR 00299 - 00200		6	03540 / 00299	
1338		BW JA,251	SHOULD NOT BRANCH		12	03546 V 03711 00251 1	
1339		BW JA,201	SHOULD NOT BRANCH		12	03558 V 03711 00201 1	
1340		SW 201,301	PLACE TWO WMS		11	03570 D 00201 00301	
1341		ZA E7,201	PUT B-A-4-2-1 BITS IN LOC 00201		11	03581 M 09571 00201	
1342		ZA E8,301			11	03592 M 09572 00301	
1343		CW 301,300			11	03603 D 00301 00300	
1344		ZA 301,300	FILL 00201 - 00299 WITH EIGHTS		11	03614 M 00301 00300	
1345		BBE JA,201,G	SHOULD NOT BRANCH		12	03625 W 03711 00201 6	
1346		BBE *E8,201,8	SHOULD BRANCH		12	03637 W 03656 00201 8	
1347		B JA			7	03649 J 03711	
1348		CS 299	TRY TO CLEAR THE EIGHTS		6	03656 / 00299	
1349	HZ	BBE JA,299,G	BRANCH IF ANY BITS AT ALL		12	03662 W 03711 00299 M	
1350		SW HZ69			6	03674 * 03671	
1351		S E1,HZ610			11	03680 S 09573 03672	
1352		CW HZ69			6	03691 D 03671	
1353		BZ JB	LEAVE ROUTINE IF NO ERROR		7	03697 J 03712 V	
1354		B H			7	03704 J 03662	
1355		JA *			1	03711 *	
1356							

PGLIN LABEL OPCODE OPERAND

CC01 CPU TEST
PAGE 11
CT ADDRS INSTRUCTION

* SUB-RTN 11.03 CHECK CLEAR STORAGE & BRANCH

1357 *
1358 *
1359 JB SW LOC * PUT SOME DATA
1360 ZA 67,100 * IN LOC 00100
1361 CS JD,100 CLEAR LOC 00100, SKIP NEXT INSTR
1362 JC B JE
1363 JD SAR HOLD1
1364 SBR HOLD1,^G SHOULD NOT BRANCH
1365 BBE JE,100,^H
1366 S EJC,HOLD1
1367 BZ *E8 SHOULD BRANCH
1368 B JE
1369 S EJC,HOLD81
1370 BZ JF SHOULD EXIT HERE
1371 JE H
1372 *****
1373 *
1374 * ROUTINE 12.00 INITIALIZE PASS COUNT WORK AREA & LOCATION 00001
1375 *
1376 JF NOPWM
1377 B *E18 SKIP NEXT TWO INSTRS WHEN SET
1378 SW *-12
1379 ZA PCC,PCCWK
1380 CS 99
1381 SW 1,8
1382 A 6RESET,6
1383 S E1,1
1384 *****
1385 *
1386 * ROUTINE 13.00 CHECK ADDRESSING BY INDEXING
1387 *
1388 * SUB-RTN 13.01 WM OVER HI-ORDER DIGIT IX REG 1
1389 JG SW X1-4
1390 ZA *X1
1391 S X1,0EX1
6 03712 Q 00100
11 03718 H 09571 00100
11 03729 / 03747 00100
7 03740 J 03816
7 03747 G 09181 A
7 03754 G 09186 B
12 03761 W 03816 00100 ^G
11 03773 S 09578 09181
7 03784 J 03798 V
7 03791 J 03816
11 03798 S 09583 09186
7 03809 J 03817 V
1 03816 .
1 03817 N
7 03818 J 03842
6 03825 Q 03818
11 03831 H 09191 09196
6 03842 / 00099
11 03848 * 00001 00008
11 03859 A 09588 00006
11 03870 S 09573 00001
6 03881 Q 00025
11 03887 H 03897 00029
11 03898 S 00029 00040

PGLIN	LABEL	CC01	CPU TEST	CT	ADRS	INSTRUCTION
1392		82	JHEX1	7	03909	J 039277 V
1393		H		1	03916	.
1394		*	SUB-RTN 13.02	SHOULD BRANCH		
1395	JH	SW	X2-4		6	03917 Q 00030
1396		ZA	*.X2		11	03923 H 03933 00034
1397		S	X2,06X2		11	03934 S 00034 000.0
1398	BZ	J16X2		SHOULD BRANCH	7	03945 J 039N3 V
1399	H				1	03952 .
1400		*	SUB-RTN 13.03		6	03953 Q 00035
1401	J1	SW	X3-4		11	03959 H 03969 00039
1402		ZA	*.X3		11	03970 S 00039 000Q
1403		S	X3,06X3		7	03981 J 039H9 V
1404	BZ	JJ6X3		SHOULD BRANCH	1	03988 .
1405	H				6	03989 Q 00040
1406		*	SUB-RTN 13.04		11	03995 H 04005 00044
1407	JJ	SW	X4-4		11	04006 S 00044 00+00
1408		ZA	*.X4		7	04017 J 04*25 V
1409		S	X4,06X4		1	04024 .
1410	BZ	JK6X4		SHOULD BRANCH	6	04025 Q 00045
1411	H				11	04031 H 04041 00049
1412		*	SUB-RTN 13.05		11	04042 S 00049 00**0
1413	JK	SW	X5-4		7	04053 J 04*W1 V
1414		ZA	*.X5		1	04060 .
1415		S	X5,06X5		6	04061 Q 00050
1416	BZ	JL6X5		SHOULD BRANCH	11	04067 H 04077 00054
1417	H				11	04078 S 00054 00*.0
1418		*	SUB-RTN 13.06		7	04089 J 04*R7 V
1419	JL	SW	X6-4		1	04096 .
1420		ZA	*.X6		6	04097 Q 00055
1421		S	X6,06X6		11	04103 H 04113 00059
1422	BZ	JM6X6		SHOULD BRANCH		
1423	H					
1424		*	SUB-RTN 13.07			
1425	JH	SW	X7-4			
1426		ZA	*.X7			

PGLIN	LABEL	CPU TEST	CC01	PAGE	13	
		OPCODE	OPERAND	CT	ADDRS	INSTRUCTION
1427		S	X7,0EX7	11	04114	S 00059 00*H0
1428		BZ	JNEX7	7	04125	J 04/C3 V
1429		H		1	04132	.
1430	* SUB-RTN 13.08			6	04133	0 00060
1431	JN	SW	X8-4	11	04139	Q H 04149 00064
1432		ZA	* , X8	11	04150	S 00064 00.00
1433		S	X8,0EX8	7	04161	J 04J69 V
1434		BZ	JPEX8	1	04168	.
1435		H		6	04169	0 00065
1436	* SUB-RTN 13.09			11	04175	Q H 04185 00069
1437	JP	SW	X9-4	11	04186	S 00069 00.00
1438		ZA	* , X9	7	04197	J 04K*5 V
1439		S	X9,0EX9	1	04204	.
1440		BZ	JQE X9	6	04205	0 00070
1441		H		11	04211	Q H 04221 00074
1442	* SUB-RTN 13.10			11	04222	S 00074 00.00
1443	JQ	SW	X1C-4	7	04233	J 04KM1 V
1444		ZA	* , X10	1	04240	.
1445		S	X1C,0EX10	6	04241	0 00075
1446		BZ	JREX10	11	04247	Q H 04257 00079
1447		H		11	04258	S 00079 00.H0
1448	* SUB-RTN 13.11			7	04269	J 04KG7 V
1449	JR	SW	X11-4	1	04276	.
1450		ZA	* , X11	6	04277	Q 00080
1451		S	X11,0EX11	11	04283	H 04293 00084
1452		EZ	JSEX11	11	04294	S 00084 00M00
1453		H		7	04305	J 04CL3 V
1454	* SUB-RTN 13.12			1	04312	.
1455	JS	SW	X12-4	6	04313	Q 00085
1456		ZA	* , X12	11	04319	H 04329 00089
1457		S	X12,0EX12	6	04320	.
1458		BZ	JTEX12	11	04329	Q 00089
1459		H		6	04330	.
1460	* SUB-RTN 13.13			11	04331	H 043329 00089
1461	JT	SW	X13-4	6	04332	Q 00085
1462		ZA	* , X13	11	04333	H 043340 00089

CC01 CPU TEST

PGLIN	LABEL	OPCODE	OPERAND	CT	ADDR	INSTRUCTION
1463	S	X13,06X13		11	04330	S 00089 00M#0
1464	BZ	JUEX13	SHOULD BRANCH	7	04341	J 04CU9 V
1465	H			1	04348	*

* SUB-RTN 13.14

1466 JV SW X14-4

1467 JU ZA *,X14

1468 S X14,06X14

1469 S X15,06X15

1470 BZ JVEX14

1471 H

* SUB-RTN 13.15

1472 JV SW X15-4

1473 JU ZA *,X15

1474 S X15,06X15

1475 KFO16X15

1476 BZ

1477 H

1478 * ROUTINE 15.00 CHECK OPERATION OF BRANCH CHARACTER EQUAL

1479 * ROUTINE 15.00

* SUB-RTN 15.01

1480 BCE KFC02,ATSIGN,9

1481 ANC NO BRANCH. SHOULD NOT BRANCH

1482 COMPARE D-MOD 9 WITH B-FLD 3 FOR LO COMPARE

ANC NO BRANCH. CHECK AAR & BAR SETTINGS

1483 SAR HOLDA2

1484 SBR HOLDB2

1485 BL *

1486 KFC2

1487 S EKFO2,HOLDA2

1488 BZ *

1489 KFO2

1490 S EPCUND,HOLD82

1491 B KFO2

1492 S EPCUND,HOLD82

1493 BZ KFC3

1494 KFO2 H

1495 * SUB-RTN 15.02

COMPARE D-MOD AT SIGN WITH B-FLD NINE

FOR HI COMPARE AND NO BRANCH.

1496 KFO3 BCE KFC4,NINE,6

1497 B *E8 SHOULD NOT BRANCH

1498 B+ *E8 SHOULD BRANCH

1499 * ROUTINE 15.03

KFC4,NINE,6

1499 B *E8 SHOULD NOT BRANCH

CC01

PAGE 14

PGLIN	LABEL	C001 CPU TEST OPCODE	C002 OPERAND	CC01 INSTRUCTION	CT	ADDRS	PAGE 15
1499		6	*68		7	04524 J 04538	
1500		B1	KFC5	SHOULD BRANCH	7	04531 J 04539 U	
1501	KF04	H			1	04538 .	
1502	*	SUB-RTN 15.03	COMPARE D-MOD AMPSAND W/B-FLD AMPSAND FOR EQ COMPARE AND BRANCH. CHECK AAR & BAR SETTINGS		12	04539 8 04558 09072 6	
1503	*				7	04551 J 04636	
1504	KF05	BCE	KF07,AMPSND,6	SHOULD BRANCH	7	04558 G 09181 A	
1505	KF06	B	KF08		7	04565 G 09186 B	
1506	KF07	SAR	HOLDA2		7	04572 J 04636 /	
1507		SBR	HOLCB2	SHOULD NOT BRANCH	7	04579 J 04593 S	
1508		BU	KF08		7	04586 J 04636	
1509		BE	*68	SHOULD BRANCH	11	04593 S 09603 09181	
1510		B	KFC8		7	04604 J 04618 V	
1511		S	EKF07,HOLDA2		7	04611 J 04636	
1512		BZ	*68		11	04618 S 09608 09186	
1513		B	KFC8		7	04629 J 04637 V	
1514		S	EKF06,HOLDB2	SHOULD BRANCH & EXIT	1	04636 .	
1515		BZ	KG		*****		
1516	KF08	H			*****		
1517					*****		
1518	*				*****		
1519	*	ROUTINE 16.00	CHECK CERTAIN MOVE OPCODES PREPARATORY TO COMPARE		*****		
1520	*	SUB-RTN 16.01	CHECK SCNL'S FOR STEPPING AAR, BAR ONE POSITION		*****		
1521		KG	CS 103		6	04637 / 00103	
1522			SCNL'S 102,103		12	04643 0 00102 00103	
1523			SAR HOLDA2		7	04655 G 09181 A	
1524			SBR HOLDB2		7	04662 G 09186 B	
1525			S 30C101A,HOLDA2	SHOULD BRANCH	11	04669 S 09613 09181	
1526		BZ	*68		7	04680 J 04694 V	
1527		B	KH		7	04687 J 04712	
1528		S 30C102A,HOLDB2	KI	SHOULD BRANCH	11	04694 S 09618 09186	
1529		BZ			7	04705 J 04713 V	
1530					1	04712 .	
1531	KH	H			*****		
1532	*	SUB-RTN 16.02	CHECK MLNS FOR CORRECT OPERATION		6	04713 / 00101	
1533	KI	CS 101			6	04719 , 00100	
1534		SW 10C					

PGIN	LABEL	CPU TEST	OPCOD	OPERAND	CT	ADDRS	INSTRUCTION
1535		Z A MINUS7,101			11	04725	Q 09108 00101
1536	MLNS	WYE,101			12	04736	D 09118 00101 1
1537	BRE	KJ,101,X			12	04748	W 04803 00101 X
1538	BW	KJ,101			12	04760	V 04803 00101 1
1539	BEE	*EE,101,-			12	04772	W 04791 00101 -
1540	B	KJ			7	04784	J 04803
1541	BEE	KK,101,8	H	EXIT HERE	12	04791	W 04804 00101 8
1542	KJ				1	04803	.
1543	*	SUB-RTN 16.03		CHECK MLZS FOR CORRECT OPERATION			
1544	KK	CS,101			6	04804	/ 00101
1545	SW	100			6	04810	G 00100
1546	Z A	MINUS8,101			11	04816	M 09109 00101
1547	MLZS	EKS,101			12	04827	D 09117 00101 2
1548	BEE	KL,101,P			12	04839	W 04894 00101 P
1549	BW	KL,101			12	04851	V 04894 00101 1
1550	BEE	*EE,101,8			12	04863	W 04882 00101 8
1551	B	KL			7	04875	J 04894
1552	BEE	KM,101,*	H		12	04882	W 04895 00101 *
1553	KL				1	04894	.
1554	*	SUB-RTN 16.04		CHECK MLCS FOR CORRECT OPERATION			
1555	KM	CS,101			6	04895	/ 00101
1556	SW	10C			6	04901	G 00100
1557	Z A	MINUS0,101			11	04907	M 09101 00101
1558	MLCS	VEE,101			12	04918	D 09115 00101 3
1559	BW	KN,101			12	04930	V 05004 00101 1
1560	BEE	KN,101,?			12	04942	W 05004 00101 :
1561	BEE	*CB,101,1			12	04954	W 04973 00101 1
1562	B	KN			7	04966	J 05004
1563	BEE	*EE,101,4			12	04973	W 04992 00101 4
1564	B	KN			7	04985	J 05004
1565	BEE	KR,101,*	H	SHOULD EXIT HERE	12	04992	W 05005 00101 *
1566	KN				1	05004	.
1567	*****	*****	*****	*****			
1568	*	ROUTINE 17.00		CHECK COMPARE OPCOD USING SINGLE CHARACTERS			
1569	*	ROUTINE 17.00					
1570	*						

PGLIN LABEL CCO1 CPU TEST
 OPCODE OPERAND

CC01 CT ADDRS INSTRUCTION
PAGE 17

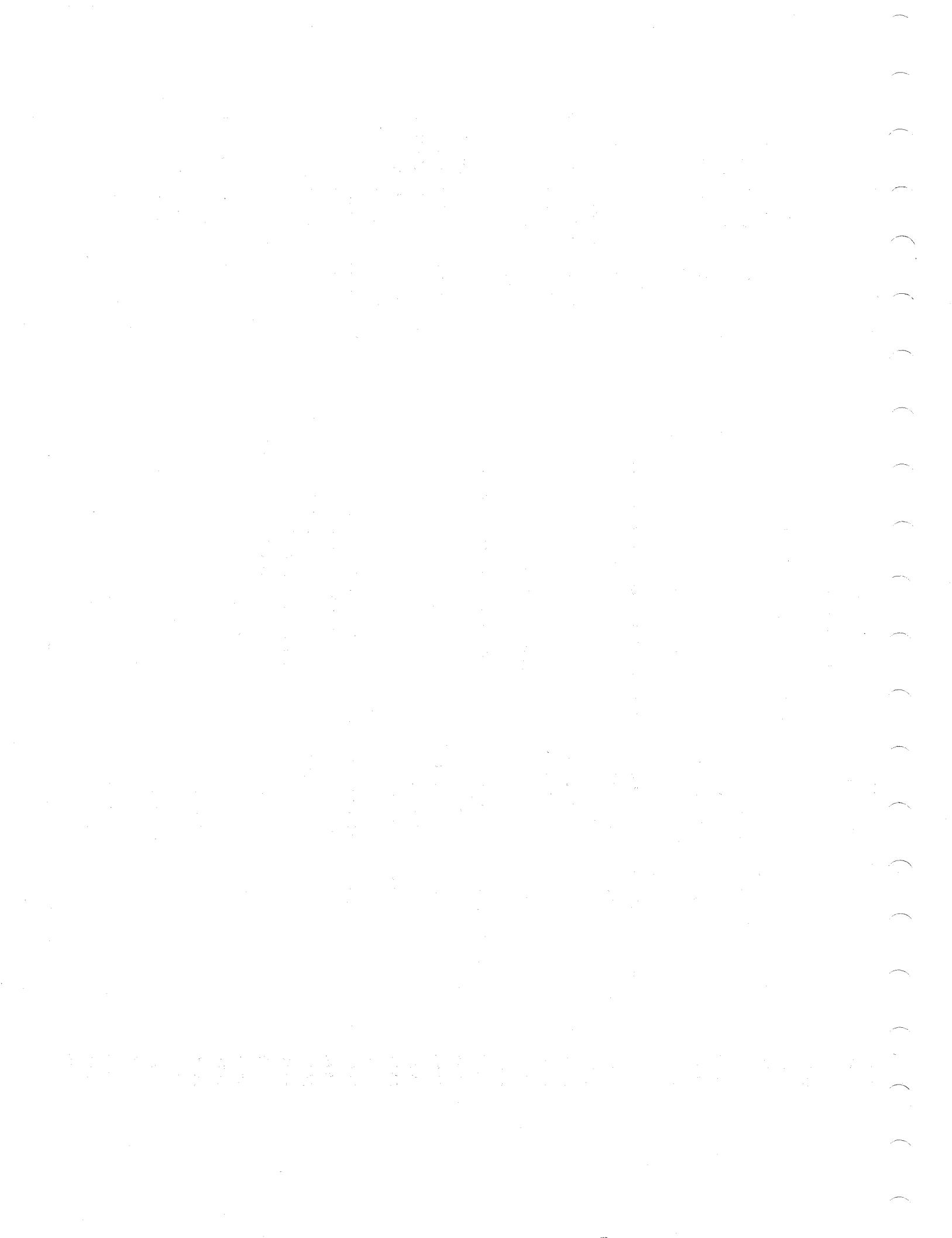
1571 * THIS ROUTINE COMPARES ALL SIXTY-FOUR LEGITIMATE
1572 * CHARACTERS WITH ONE ANOTHER AND INSURES THAT ALL
1573 * IDENTICAL CHARACTERS COMPARE EQUAL. THAT NO
1574 * CHARACTER COMPARES EQUAL TO ANY CHARACTER EXCEPT
1575 * ITSELF. AND THAT THE COLLATING SEQUENCE IS PROPER

1576 *
1577 *
1578 *
1579 * BEGIN BY USING SIMPLEST COMPARISONS TO VERIFY
1580 * CORRECT OPERATION OF BRANCH HI, LO, EQ, UNEQUAL

1581 * SUB-RTN 17.01 COMPARE A-FLD 9 WITH B-FLD 3 FOR LO COMPARE
1582 KR C NINE,ATSIGN
1583 BE KS SHOULD NOT BRANCH
1584 BU *68 SHOULD BRANCH
1585 B KS SHOULD NOT BRANCH
1586 BF *68 SHOULD BRANCH
1587 BL KT SHOULD BRANCH
1588 KS H H
1589 * SUB-RTN 17.02 COMPARE A-FLD 3 WITH B-FLD 9 FOR HI COMPARE
1590 KT C ATSIGN,NINE
1591 BE KU SHOULD NOT BRANCH
1592 BU *68 SHOULD BRANCH
1593 B KU SHOULD NOT BRANCH
1594 BL KU SHOULD BRANCH
1595 BF KV KV
1596 KU H H
1597 * SUB-RTN 17.03 COMPARE AMPERSAND WITH AMPERSAND FOR EQ COMPARE
1598 KV C AMPSND,AMPSND
1599 BU KW SHOULD
1600 BF KW NOT
1601 BL KW BRANCH
1602 BE *62 SHOULD BRANCH
1603 KW H
1604 * ROUTINE 19.00 CHECK OPERATION OF DATA MOVE INSTRUCTION
1605 *

11606	* SUB-RTN 19.01 CHECK SCNL'S FOR MOVE NO DATA									
11607	LK	MLCS	NWM63,WORK6							
11608		SW	WORK6	6	05151	*	09176			
11609	SCNL'S	NWM00,WORK6		12	05157	D	09002	09177		
11610	C	ALLBIT,WORK6		11	05169	C	09071	09177		
11611	BE	LL	SHOULD BRANCH	7	05180	J	05188	S		
11612	H			1	05187	*				
11613	* SUB-RTN 19.02 CHECK MLNS FOR MOVE NUMERIC, NO ZONES, NO WM									
11614	LL	MLCS	NWM62,WORK6	12	05188	D	09063	09177		
11615	SW	WORK6		6	05200	*	09176			
11616	MLNS	NWM01,WORK6		12	05206	D	09003	09177		
11617	C	AYE,WORK6		11	05218	C	09092	09177		
11618	BE	LM	SHOULD BRANCH	7	05229	J	05237	S		
11619	H			1	05236	*				
11620	* SUB-RTN 19.03 CHECK MLZS FOR MOVE ZONES, NO NUMERIC, NO WM									
11621	LH	MLCS	NWM31,WORK6	12	05237	D	09032	09177		
11622	SW	WORK6		6	05249	*	09176			
11623	MLZS	NWM32,WORK6		12	05255	D	09033	09177		
11624	C	DELTA,WORK6		11	05267	C	09077	09177		
11625	BE	LN	SHOULD BRANCH	7	05278	J	05286	S		
11626	H			1	05285	*				
11627	* SUB-RTN 19.04 CHECK MLCS FOR MOVE NUMERIC, ZONE, NO WM									
11628	LN	MLNS	NWM25,WORK6	12	05286	D	09027	09177		
11629	MLZS	NWM25,WORK6		12	05298	D	09027	09177		
11630	SW	WORK6		6	05310	*	09176			
11631	MLCS	NWM38,WORK6		12	05316	D	09039	09177		
11632	C	OH,WORK6		11	05328	C	09107	09177		
11633	BE	LP	SHOULD BRANCH	7	05339	J	05347	S		
11634	H			1	05346	*				
11635	* SUB-RTN 19.05 CHECK MLWS FOR MOVE WM, NO ZONE, NO NUMERIC									
11636	LP	MLCS	NWM63,WORK6	12	05347	D	09064	09177		
11637	CW	WORK6		6	05359	D	09176			
11638	MLWS	BLANK,WORK6		12	05365	D	09066	09177		
11639	C	ALLBIT,WORK6		11	05377	C	09071	09177		
11640	BE	LQ	SHOULD BRANCH	7	05388	J	05396	S		
11641	H			1	05395	*				
11642	* SUB-RTN 19.06 CHECK MLWS FOR MOVE NUMERIC, WM, NO ZONE									
11643	LQ	MLCS	NWM54,WORK6	12	05396	D	09056	09177		

1645	PLNWS	NINE,WORK6			12	05414	D 09129 09176 5
1646	C	EYE,WORK6			11	05426	C 09100 09176
1647	BE	LR	SHOULD BRANCH		7	05437	J 05445 S
1648	H				1	05444	.
1649	*	SUB-RTN 19.07	CHECK MLZWS FOR MOVE ZONE. WM. NO NUMERIC		12	05445	D 09032 09176 3
1650	LR	MLCS	NWM31,WORK6		6	05457	□ 09176
1651		CW	WORK6		12	05463	D 09078 09176 6
1652		MLZWS	DASH,WORK6		11	05475	C 09077 09176
1653		C	DELTA,WORK6	SHOULD BRANCH	7	05486	J 05494 S
1654		BE	LS		1	05493	.
1655		H			12	05494	D 09002 09176 3
1656	*	SUB-RTN 19.08	CHECK MLCWS FOR MOVE CHARACTER AND WORD MARK		6	05506	□ 09176
1657	LS	MLCS	NWM00,WORK6		12	05512	D 09071 09176 7
1658		CW	WORK6		11	05524	C 09071 09176
1659		MLCWS	ALLBIT,WORK6		7	05535	J 05543 S
1660		C	ALLBIT,WORK6	SHOULD BRANCH	1	05542	.
1661		BE	LT		12	05543	D 09064 00100 7
1662		H			12	05555	D 09066 00101 7
1663	*	SUB-RTN 19.09	CHECK SCNR FOR MOVE NO DATA. PROPER ADDR REG STEP		12	05567	D 00100 00101 8
1664	LT	MLCWS	NWM63,100		7	05579	G 09181 A
1665		MLCWS	BLANK,101		7	05586	G 09186 B
1666		SCNR	LOC,101		11	05593	C 09181 09613
1667		SAR	HOLDA2		7	05604	J 05709 /
1668		SBR	HOLDB2		11	05611	C 09186 09618
1669		C	HOLDA2,00010101	CK AAR FOR PROPER STEPPING	7	05622	J 05709 /
1670		BU	LU	SHOULD NOT BRANCH	11	05629	C 09066 00101
1671		C	HOLDB2,00010201	CK BAR FOR PROPER STEPPING	7	05640	J 05709 /
1672		BU	LU	SHOULD NOT BRANCH	12	05647	D 00101 00100 8
1673		C	BLANK,101	TEST LOC 00101 FOR WM-BLANK	7	05659	G 09181 A
1674		BU	LU	SHOULD NOT BRANCH	7	05666	G 09186 B
1675		SCNR	101,100		11	05673	C 09181 09618
1676		SAR	HOLDA2		7	05684	J 05709 /
1677		SBR	HOLDB2	CK AAR FOR PROPER STEPPING	11	05691	C 09186 09613
1678		C	HOLDA2,00010201	SHOULD NOT BRANCH	7	05702	J 05710 S
1679		BU	LU	CK BAR FOR PROPER STEPPING	1	05709	.
1680		C	HOLDB2,00010101	SHOULD BRANCH & EXIT	12	05710	D 09051 09176 7
1681		BE	LV				
1682	LU	H					
1683	*	SUB-RTN 19.10	CHECK MRN SIMILAR TO MLNS				
1684	LV	MLCWS	NWM50,WORK6				



CC01	CPU TEST	CC01	PAGE			
GLIN	LABEL	OPCODE	OPERAND	CT	ADDRS	INSTRUCTION
685		MRN	COLON, WORK6		12	05722 D 09088 09176 9
1686		BW	*E13, WORK6		12	05734 V 05758 09176 1
1687		BCE	LW, WORK6, B		12	05746 B 05759 09176 B
1688	H				1	05758 .
1689	*	SUB-RTN 19.11	CHECK MRZ		12	05759 D 09048 09176 7
1690	LW	MLCWS	NW#47, WORK6		12	05771 D 09085 09176 0
1691		MRZ	SUELNK, WORK6		12	05783 V 05807 09176 1
1692		BW	*E13, WORK6		12	05795 B 05808 09176 M
1693		BCE	LX, WCRK6, M		1	05807 .
1694	H					
1695	*	SUB-RTN 19.12	CHECK MRC		12	05808 D 09014 09176 7
1696	LX	MLCWS	NW#12, WORK6		12	05820 D 09094 09176 #
1697		MRC	SEE, WORK6		12	05832 V 05856 09176 1
1698		BW	*E13, WORK6		12	05844 B 05857 09176 C
1699		BCE	LY, WORK6, C		1	05856 .
1700	H					
1701	*	SUB-RTN 19.13	CHECK PRW		12	05857 D 09071 09176 7
1702	LY	MLCWS	ALLBIT, WORK6		12	05869 D 09002 09176 3
1703		MRW	NW#00, WORK6		12	05881 V 05905 09176 1
1704		BW	*E13, WORK6		12	05893 B 05906 09176 G
1705		BCE	LZ, WORK6, G		1	05905 .
1706	H					
1707	*	SUB-RTN 19.14	CHECK MRNW		12	05906 D 09091 09176 7
1708	LZ	MLCWS	QUESTN, WORK6		12	05918 D 09007 09176 .
1709		MRNW	NW#05, WORK6		12	05930 V 05954 09176 1
1710		BW	*E13, WORK6		12	05942 B 05955 09176 E
1711		BCE	MA, WORK6, E		1	05954 .
1712	H					
1713	*	SUB-RTN 19.15	CHECK MRZW		12	05955 D 09090 09176 7
1714	PA	MLCWS	TPPARK, WORK6		12	05967 D 09049 09176 G
1715		MRZW	NW#48, WORK6		12	05979 V 06003 09176 1
1716		BW	*E13, WORK6		12	05991 B 06004 09176 M
1717		BCE	MB, WORK6, M		1	06003 .
1718	H					
1719	*	SUB-RTN 19.16	CHECK MRCW			

CPU TEST
OPCODE OPERAND

PGIN

LABEL

CT ADDRS INSTRUCTION

1720	MB	MLCWS	EPM, WORK6	12	06004	D 09105 09176 7
1721	MRCW	NWM27, WORK6		12	06016	D 09028 09176 M
1722	BW	*E13, WORK6	SHOULD NOT BRANCH	12	06028	V 06052 09176 1
1723	BCE	MC, WORK6,,	SHOULD BRANCH	12	06040	B 06053 09176 .
1724	H			1	06052	.
1725	*	SUB-RTN 19.17	CHECK SCNLA FOR MOVE NO DATA, PROPER ADDR REG STP	12	06053	D 09069 00102 7
1726	MC	MLCWS	LBRAKT, 102	12	06065	D 09004 00103 7
1727		MLCWS	NWM02, 103	12	06077	D 09069 00104 7
1728		MLCWS	LBRAKT, 104	12	06089	D 00103 00104 S
1729		SCNLA	103, 104	7	06101	G 09181 A
1730		SAR	HOLDA2	7	06108	G 09186 B
1731		SBR	HOLD82	11	06115	C 09181 09613
1732		C	HOLDA2, 000101a	11	06115	C 09186 09618
1733		BU	MD	7	06126	J 06169 /
1734		C	HOLD82, 000102a	11	06133	C 09186 09618
1735		BU	MD	7	06144	J 06169 /
1736		C	NWM61, 104	11	06151	C 09062 00104
1737	PD	BE	ME	7	06162	J 06170 S
1738	H			1	06169	.
1739	*	SUB-RTN 19.18	CHECK MLNA	12	06170	D 09077 00102 7
1740	ME	MLCWS	DELTA, 102	12	06182	D 09018 00103 7
1741		MLCWS	NWM16, 103	12	06194	D 09077 00104 7
1742		MLCWS	DELTA, 104	12	06206	D 00103 00104 /
1743		MLNA	103, 104	11	06218	C 09033 00104
1744		C	NWM32, 104	7	06229	J 06237 S
1745		BE	MF	1	06236	.
1746	H					
1747	*	SUB-RTN 19.19	CHECK MLZA	12	06237	D 09081 00102 7
1748	MF	MLCWS	PERCNT, 102	12	06249	D 09036 00103 7
1749		MLCWS	NWM35, 103	12	06261	D 09081 00104 7
1750		MLCWS	PERCNT, 104	12	06273	D 00103 00104 S
1751		MLZA	103, 104	11	06285	C 09045 00104
1752		C	NWM44, 104	7	06296	J 06304 S
1753	BE	MG		1	06303	.
1754	H					

PGLIN	LABEL	CPU TEST	OPCOD	OPERAND	CC01	PAGE	21
					CT	ADDRS	INSTRUCTION
1755	*	SUB-RTN 19.20	CHECK MLC A				
1756	M G	MLCWS	NWM63,WORK6		12	06304	D 09064 09176 7
1757		MLCA	BLANK,WORK6		12	06316	D 09066 09176 1
1758		BW	*E13,WORK6	SHOULD NOT BRANCH	12	06328	V 06352 09176 1
1759		BCE	MH,WORK6,	SHOULD BRANCH	12	06340	B 06353 09176
1760	H				1	06352	*
1761	*	SUB-RTN 19.21	CHECK MLWA				
1762	M H	MLCWS	NWM53,WORK6		12	06353	D 09054 09176 7
1763		MLWA	NAUGHT,WORK6		12	06365	D 09120 09176 0
1764		C	NWM53,WORK6		11	06377	C 09054 09176
1765		BE	M1	SHOULD BRANCH	7	06388	J 06396 S
1766	H				1	06395	*
1767	*	SUB-RTN 19.22	CHECK MLNWA				
1768	M I	MLCWS	NWM47,WORK6		12	06396	D 09048 09176 7
1769		MLNWA	SUBLNK,WORK6		12	06408	D 09085 09176 V
1770		C	NWM32,WORK6		11	06420	C 09033 09176
1771		BE	M J	SHOULD BRANCH	7	06431	J 06439 S
1772	H				1	06438	*
1773	*	SUB-RTN 19.23	CHECK MLZWA				
1774	M J	MLCWS	NWM03,WORK6		12	06439	D 09005 09176 7
1775		MLZWA	LOZNGE,WORK6		12	06451	D 09068 09176 W
1776		C	NWM51,WORK6		11	06463	C 09052 09176
1777		BE	M K	SHOULD BRANCH	7	06474	J 06482 S
1778	H				1	06481	*
1779	*	SUB-RTN 19.24	CHECK MLCWA				
1780	M K	MLCWS	ALLBIT,102		12	06482	D 09071 00102 7
1781		MLCWS	NWM00,103		12	06494	D 09002 00103 7
1782		MLCWS	ALLBIT,104		12	06506	D 09071 00104 7
1783		MLCWA	103,104		12	06518	D 00103 00104 X
1784		BW	*E13,104	SHOULD NOT BRANCH	12	06530	V 06554 00104 1
1785		BCE	ML,104,	SHOULD BRANCH	12	06542	B 06555 00104
1786	H				1	06554	*
1787	*	SUB-RTN 19.25	CHECK SCNRR FOR MOVE NO DATA, PROPER ADDR REG STP				
1788	M L	MLCWA	NWM26,101		12	06555	D 09065 00101 X
1789		MLCWS	GREATR,37		12	06567	D 09089 00037 7

CC01 CPU TEST
OPCOD OPERAND

CC01 PAGE 22
CT ADDRS INSTRUCTION

1790	MLCWS	NWM49,36		12	06579	D 09050 00036 7
1791	SCNRR	37,36		12	06591	D 00037 00036 Y
1792	SAR	HOLDA2		7	06603	G 09181 A
1793	SBR	HOLDB2		7	06610	G 09186 B
1794	C	HOLDA2,000102a	CHECK AAR FOR PROPER STEPPING	11	06617	C 09181 09618
1795	MM		SHOULD NOT BRANCH	7	06628	J 06677 /
1796	C	HOLDB2,000101a	CHECK BAR FOR PROPER STEPPING	11	06635	C 09186 09613
1797	BU	MM	SHOULD NOT BRANCH	7	06646	J 06677 /
1798	SW	38		6	06653	* 00038
1799	C	NWM26,101	TEST THAT NO DATA WERE MOVED	11	06659	C 09065 00101
1800	BE	MN	SHOULD BRANCH & EXIT	7	06670	J 06678 S
1801	MN	H		1	06677	*
1802	*	SUB-RTN 19.26	CHECK MRNR			
1803	MN	CW	10C	6	06678	H 00100
1804		MRCW	K01,100	12	06684	D 09130 00100 H
1805		MRNR	K02,100	12	06696	D 09132 00100 Z
1806		BW	MP,100	12	06708	V 06770 00100 1
1807		BW	*E8,101	12	06720	V 06739 00101 1
1808		B	MP	7	06732	J 06770
1809		BCE	*E8,100,	12	06739	B 06758 00100
1810		B	MP	7	06751	J 06770
1811		BCE	MQ,101,0	12	06758	B 06771 00101 *
1812		MP	H	1	06770	*
1813	*	SUB-RTN 19.27	CHECK MRZR			
1814	MQ	CW	100	6	06771	H 00100
1815		MRCW	KC3,100	12	06777	D 09134 00100 H
1816		MRZR	K04,100	12	06789	D 09136 00100 *
1817		BW	MR,100	12	06801	V 06863 00100 1
1818		BW	*E8,101	12	06813	V 06832 00101 1
1819		B	MR	7	06825	J 06863
1820		BCE	*E8,100,-	12	06832	B 06851 00100 -
1821		B	MR	7	06844	J 06863
1822		BCE	MS,101,V	12	06851	B 06864 00101 V
1823		MR	H	1	06863	*
1824	*	SUB-RTN 19.28	CHECK MRCR			

CC01 CPU TEST
OPCODE OPERAND

CC01 PAGE 23

PCLIN	LABEL	CT	ADDRS	INSTRUCTION
1825	MS	MLCWA	K05,101	
1826		MRCR	K06,100	
1827		BW	*E8,100	SHOULD BRANCH
1828		B	PT	
1829		C	101,K1461	
1830		BE	MJ	SHOULD BRANCH & EXIT
1831	MT	H		
1832	*	SUB-RTN	19.29	CHECK MRWR
1833	MU	MLCWA	K07,101	
1834		MRWR	K08,100	SHOULD NOT BRANCH
1835		BW	MV,100	SHOULD BRANCH
1836		BW	*E8,101	
1837		B	MV	SHOULD BRANCH
1838		BCE	*E8,100,I	
1839		B	MV	SHOULD BRANCH
1840		BCE	MW,101,N	SHOULD BRANCH & EXIT
1841	MV	H		
1842	*	SUB-RTN	19.30	CHECK MRNWR
1843	MW	MLCWA	K09,101	
1844		MRNWR	K1C,100	SHOULD NOT BRANCH
1845		BW	MX,100	SHOULD BRANCH
1846		BW	*E8,101	
1847		B	MX	SHOULD BRANCH
1848		BCE	*E8,100,S	
1849		B	MX	SHOULD BRANCH
1850		BCE	MY,101,?	
1851	NX	H		
1852	*	SUB-RTN	19.31	CHECK MRZWR
1853	NY	MLCWA	K11,101	
1854		MRZWR	K12,100	SHOULD NOT BRANCH
1855		BW	MZ,100	SHOULD BRANCH
1856		BW	*E8,101	
1857		B	MZ	SHOULD BRANCH
1858		BCE	*E8,100,X	
1859		B	MZ	

12	06864	D 09139 00101 X
12	06876	D 09140 00100 *
12	06888	V 06907 00100 1
7	06900	J 06925
11	06907	C 00101 09157
7	06918	J 06926 S
1	06925	*
12	06926	D 09143 00101 X
12	06938	D 09144 00100 X
12	06950	V 07012 00100 1
12	06962	V 06981 00101 1
7	06974	J 07012
12	06981	B 07000 00100 1
7	06993	J 07012
12	07000	B 07013 00101 N
1	07012	*
12	07013	D 09147 00101 X
12	07025	D 09148 00100 S
12	07037	V 07099 00100 1
12	07049	V 07068 00101 1
7	07061	J 07099
12	07068	B 07087 00100 S
7	07080	J 07099
12	07087	B 07100 00101 *
1	07099	*
12	07100	D 09151 00101 X
12	07112	D 09152 00100 S
12	07124	V 07186 00100 1
12	07136	V 07155 00101 1
7	07148	J 07186
12	07155	B 07174 00100 X
7	07167	J 07186

PGLIN	LABEL	CPU TEST	OPCODE	OPERAND	SHOULD BRANCH & EXIT	12	07174	B 07187 00101 V
1860		BCE	NA,101,V	H		1	07186	*
1861	RZ	* SUB-RTN 19.32	CHECK MRCWR			6	07187	□ 00100
1862	NA	CW	100			12	07193	D 09154 00100 T
1863		MRCW	K13,100			12	07205	D 09156 00100 S
1864		MRCWR	K14,100			12	07217	V 07236 00100 H
1865		BW	*C8,100	SHOULD BRANCH		7	07229	J 07254
1866		NB				11	07236	C 00101 09157
1867		B				11	07247	J 07255 S
1868		C	101,K1461			1	07254	*
1869		AE	NC	SHOULD BRANCH & EXIT				
1870	R8	H						
1871		* SUB-RTN 19.33	CHECK SCNLB FOR MOVE NO DATA, PROPER ADDR REG STP			12	07255	D 09090 00102 7
1872	NC	MLCWS	TPMARK,1C2			12	07267	0 09049 00103 7
1873		MLCWS	NWM48,103			12	07279	D 09072 00104 7
1874		MLCWS	AMPSND,104			12	07291	D 00104 00103 -
1875		SCNLB	104,103			7	07303	G 09181 A
1876		SAR	HOLDZ2			7	07310	G 09186 B
1877		SBR	HOLDZ2			11	07317	C 09181 09618
1878		C	HOLDZ2,000102A		SHOULD NOT BRANCH	7	07328	J 07371 /
1879		BU	ND			11	07335	C 09186 09613
1880		C	HOLDZ2,000101A			7	07346	J 07371 /
1881		BU	ND	SHOULD NOT BRANCH		11	07353	C 09017 00102
1882		C	NWM15,102	TEST THAT NO DATA WERE MOVED		7	07364	J 07372 S
1883		BE	NE	SHOULD BRANCH & EXIT		1	07371	*
1884	NO	H						
1885		* SUB-RTN 19.34	CHECK MLNB			12	07372	D 09083 09176 7
1886	NE	MLCWS	BKSLSH,WORK6			12	07384	D 09034 09176 J
1887		MLNB	NWM33,WORK6			11	07396	C 09019 09176
1888		C	NWM17,WORK6		SHOULD BRANCH	7	07407	J 07415 S
1889		BE	NF			1	07414	*
1890		H						
1891		* SUB-RTN 19.35	CHECK MLZB			6	07415	* 00100
1892	NF	SW	10C			12	07421	D 09064 00101 7
1893		MLCWS	NWM63,101			12	07433	D 09066 00101 K
1894		MLZB	BLANK,101					

CC01 CPU TEST
OPCOD OPERAND

PGLIN	LABEL	CPU TEST	OPCOD	OPERAND	CT	ADDRS	INSTRUCTION
1895		BW	*E13,1C1		12	07445	V 07469 00101 1
1896		BCE	NG,101,M		12	07457	B 07470 00101 M
1897	H				1	07469	*
1898	* SUB-RTN 19.36	CHECK MLCB			6	07470	*
1899	NG	SW	10C		12	07476	D 09053 00101 7
1900		MLCWS	NWM52,101		12	07488	D 09086 00101 L
1901		MLCB	POUND,101		12	07500	V 07524 00101 1
1902	BW	*E13,1C1			12	07512	B 07525 00101 *
1903	BCE	NH,101,M			1	07524	*
1904	H				6	07525	*
1905	* SUB-RTN 19.37	CHECK MLWB			12	07531	D 09017 00101 7
1906	NH	SW	10C		12	07543	D 09072 00101 M
1907		MLCWS	NWM15,101		11	07555	C 09017 00101
1908		MLWB	AMPSND,101		7	07566	J 07574 S
1909	C	NWM15,101			1	07573	*
1910	BE	NJ			6	07574	*
1911	H				12	07580	D 09008 00101 7
1912	*SUB-RTN 19.38	CHECK MLNWB			12	07592	D 09100 00101 N
1913	NJ	SW	10C		11	07604	C 09011 00101
1914		MLCWS	NWM06,101		7	07615	J 07623 S
1915		MLNWB	EYE,101		1	07622	*
1916	C	NWM09,101			12	07623	D 09071 09176 7
1917	BE	NJ			12	07635	D 09002 09176 0
1918	H				12	07647	V 07671 09176 1
1919	* SUB-RTN 19.39	CHECK MLZWB			12	07659	B 07672 09176 M
1920	NJ	MLCWS	ALLBIT,WORK6		1	07671	*
1921		MLZWB	NWM00,WORK6		12	07684	D 09005 09176 P
1922	BW	*E13,WORK6			12	07696	V 07720 09176 1
1923	BCE	NK,WORK6,M			12	07708	B 07721 09176 3
1924	H				12	07672	D 09068 09176 7
1925	* SUB-RTN 19.40	CHECK MLCWB			12	07684	D 09005 09176 P
1926	NK	MLCWS	LOZNGE,WORK6		12	07696	V 07720 09176 1
1927		MLCWB	NWM03,WORK6		12	07708	B 07721 09176 3
1928	BW	*E13,WORK6			12	07708	B 07721 09176 3
1929	BCE	NL,WORK6,3			12	07708	B 07721 09176 3

PGLIN	LABEL	1930	H	1931 * SUB-RTN 19.41	CHECK SCNRG FOR MOVE NO DATA. PROPER ACDR REG STP	1932 NL	CS 164	INSURE 00100-00164 BLANK	1933	MLCWS ALLBIT,101	PUT TERMINAL CHARACTER IN 00101	1934	MLWA 164,100	INSURE NO WMS 00038-00100	1935	MLCWB NINE,100	MOVE 64 CHARACTERS TO 00037-00100	1936	CW 42	REMOVE WM FROM GROUP MARK	1937	SCNRG 37,36	TRY THE SCAN	1938	SAR HOLDA2		1939	SBR HOLDB2		1940	C HOLDA2,AC0102A	CHECK AAR FOR PROPER SETTING	1941	AU NM	SHOULD NOT BRANCH	1942	C HOLDB2,AC00101A	CHECK BAR FOR PROPER SETTING	1943	BU NM	SHOULD NOT BRANCH	1944	BW NM,42	SHOULD NOT BRANCH	1945	MLWA 164,100	REMOVE ALL WMS FROM 00038-00100	1946	MLCB NINE,164	MOVE 64 CHARACTERS TO 00101-00164	1947	C 100,164	CHECK THAT SCAN MOVED NO DATA	1948	BE NN	SHOULD BRANCH	1949 NM	H		1950 * SUB-RTN 19.42	CHECK MRNG	1951 NN	MLCWS NW#19,101		1952	MLCWS SPLAT,102		1953	MLCWS ALLBIT,103		1954	MRNG 102,101		1955	BW *E13,101	SHOULD NOT BRANCH	1956	BCE NP,101,%		1957	H		1958 * SUB-RTN 19.43	CHECK MRZG	1959 NP	MLCWS ALLBIT,101		1960	MLCWS NW#00,102		1961	MLCWS ALLBIT,103		1962	MRZG 102,101		1963	C NW#15,101	SHOULD BRANCH	1964	BE NQ																												
		1	07720	*		6	07721	/ 00164		12	07727	0 09071 00101 7		12	07739	D 00164 00100 U		12	07751	D 09129 00100 P		6	07763	□ 00042		12	07769	D 00037 00036 Q		7	07781	G 09181 A		7	07788	G 09186 B		11	07795	C 09181 09618		7	07806	J 07885 /		11	07813	C 09186 09613		7	07824	J 07885 /		12	07831	V 07885 00042 1		12	07843	D 00164 00100 U		12	07855	D 09129 00164 L		11	07867	C 00100 00164		7	07878	J 07886 S		1	07885	.		12	07886	D 09021 00101 7		12	07898	D 09074 00102 7		12	07910	D 09071 00103 7		12	07922	D 00102 00101 R		12	07934	V 07958 00101 1		12	07946	B 07959 00101 Z		1	07958	.		12	07959	D 09071 00101 7		12	07971	D 09002 00102 7		12	07983	D 09071 00103 7		12	07995	D 00102 00101 .		11	08007	C 09017 00101		7	08018	J 08026 S	

PGLIN CPU TEST
LABEL OPCODE OPERAND

PGLIN	LABEL	OPCODE	OPERAND	CT	ADDRS	INSTRUCTION
1965	H			1	08025	*
1966	* SUB-RTN 19.44		CHECK MRCG	12	08026	D 09099 00101 7
1967	NQ	MLCWS	ATTCH.101	12	08038	D 09009 00102 7
1968		MLCWS	NWM07,102	12	08050	D 09071 00103 7
1969		MLCWS	ALLBIT,1C3	12	08062	D 00102 00101 S
1970		MRCG	102,101	11	08074	C 09009 00101
1971	C	NWM07,101	SHOULD BRANCH	7	08085	J 08093 S
1972	BE	NR		1	08092	*
1973	H			12	08093	D 09077 00101 7
1974	* SUB-RTN 19.45		CHECK MRWG	12	08105	D 09018 00102 7
1975	NR	MLCWS	DELTA.101	12	08117	D 09071 00103 7
1976		MLCWS	NWM16,102	12	08129	D 00102 00101 *
1977		MLCWS	ALLBIT,1C3	12	08141	V 08165 00101 1
1978		MRWG	102,101	12	08153	B 08166 00101 D
1979	BW	*E13,101	SHOULD NOT BRANCH	1	08165	*
1980	BCE	NS,101,L		12	08202	D 00102 00101 B
1981	H			12	08214	V 08238 00101 1
1982	* SUB-RTN 19.46		CHECK MRNWG	12	08226	B 08239 00101 N
1983	NS	MLCWS	EXCLAM.101	1	08238	*
1984		PLCWS	NWM21,102	12	08178	D 09023 00102 7
1985		MLCWS	ALLBIT,103	12	08190	D 09071 00103 7
1986		MRNWG	102,101	12	082263	D 09071 00103 7
1987	BW	*E13,101	SHOULD NOT BRANCH	12	08275	D 00102 00101 :
1988	BCE	NT,101,N	SHOULD BRANCH	11	08287	C 09017 00101
1989	H			7	08298	J 08306 S
1990	* SUB-RTN 19.47		CHECK MRZWG	1	08305	*
1991	NT	MLCWS	NWM63,101	12	08239	D 09064 00101 7
1992		MLCWS	BLANK,102	12	08251	D 09066 00102 7
1993		PLCWS	ALLBIT,103	12	08263	D 09071 00103 7
1994		MRZWG	102,101	12	08275	D 00102 00101 :
1995	C	NWM15,101	SHOULD BRANCH	7	08298	J 08306 S
1996	BE	NU		1	08305	*
1997	H			12	08306	D 09049 00101 7
1998	* SUP-RTN 19.48		CHECK MRCWG			
1999	NU	MLCWS	NWM48,101			

PGLIN	LABEL	OPCODE	OPERAND	C	ADDRS	INSTRUCTION
2000		MLCWS	TPWARK,102	12	08318	D 09090 00102 7
2001		MLCWS	ALLBIT,103	12	08330	D 09071 00103 7
2002		MRCWG	102,101	12	08342	D 00102 00101 L
2003		C	NW#15,101	11	08354	C 09017 00101
2004		BE	NV	7	08365	J 08373 S
2005	H			1	08372	*
2006	* SUB-RTN 19.49		CHECK SCNL FOR MOVE NO DATA, PROPER ADDR REG STEP	12	08373	D 09102 00102 7
2007	NW	MLCWS	JAY,102	12	08385	D 09031 00103 7
2008		MLCWS	NWM30,103	12	08397	D 00102 00103 6
2009		SCNL	102,103	7	08409	G 09181 A
2010		SAR	HOLDA2	7	08416	G 09186 B
2011		SBR	HOLCB2	11	08423	C 09181 09613
2012	C	HOLDA2,a00101a	CHECK AAR FOR PROPER STEPPING	7	08434	J 08552 /
2013	BU	NW	SHOULD NOT BRANCH	11	08441	C 09186 09618
2014	C	HOLDB2,a00102a	CHECK BAR FOR PROPER STEPPING	7	08452	J 08552 /
2015	BU	NW	SHOULD NOT BRANCH	7	08459	V 08552 00103 1
2016	BK	NW,103	SHOULD NOT BRANCH WORD MARK	12	08471	B 08490 00103 8
2017	BCE	*E8,103,S	SHOULD BRANCH	7	08483	J 08552
2018	B	NW	TEST STOP ON B-FIELD NW	12	08490	D 00103 00102 6
2019	SCNL	103,102		7	08502	G 09181 A
2020	SAR	HOLDA2		7	08509	G 09186 B
2021	SBR	HOLDB2		11	08516	C 09181 09618
2022	C	HOLDA2,a00102a	SHOULD NOT BRANCH	7	08527	J 08552 /
2023	BU	NW	SHOULD BRANCH & EXIT	11	08534	C 09186 09613
2024	C	HOLCB2,a00101a		7	08545	J 08553 S
2025	BE	NX		1	08552	*
2026	NW	H				
2027	* SUB-RTN 19.50		CHECK MLN	12	08553	D 09064 09176 7
2028	NX	MLCWS	NWM63,WORK6	12	08565	D 09066 09176 A
2029		MLN	BLANK,WORK6	12	08577	V 08601 09176 1
2030		BW	*E13,WORK6	12	08589	B 08602 09176 E
2031		BCE	NY,WORK6,E	1	08601	*
2032	H					
2033	* SUB-RTN 19.51		CHECK MLZ	12	08602	D 09052 09176 7
2034	NV	MLCWS	NWM51,WORK6			

CC01 CPU TESTI
OPCODE OPERAND

CT ADDRS INSTRUCTION

PGLIN	LABEL	MLZ	ATSIGN,WORK6	SHOULD NOT BRANCH	12 08614 D 09087 09176 A
2035		BW	*E13,WORK6		12 08626 V 08650 09176 1
2036		BCE	NZ,WORK6,3	SHOULD BRANCH	12 08638 B 08651 09176 3
2038		H			1 08650 *
2039	* SUB-RTN 19.52		CHECK MLC		
2040	NZ	MLCWS	NWM31,WORK6		12 08651 D 09032 09176 7
2041		MLC	DASH,WORK6		12 08663 D 09078 09176 C
2042	BW		*E13,WORK6	SHOULD NOT BRANCH	12 08675 V 08699 09176 1
2043		BCE	PA,WORK6,-	SHOULD BRANCH	12 08687 B 08700 09176 -
2044		H			1 08699 *
2045	* SUB-RTN 19.53		CHECK MLW		
2046	PA	MLCWS	NWM09,WORK6		12 08700 D 09011 09176 7
2047		MLW	EFF,WORK6		12 08712 D 09097 09176 D
2048		C	NWM09,WORK6		11 08724 C 09011 09176
2049		BE	PB	SHOULD BRANCH	7 08735 J 08743 S
2050		H			1 08742 *
2051	* SUB-RTN 19.54		CHECK MLNW		
2052	PB	MLCWS	ALLBIT,WORK6		12 08743 D 09071 09176 7
2053		MLNW	NWM00,WORK6		12 08755 D 09002 09176 E
2054	BW		*E13,WORK6	SHOULD NOT BRANCH	12 08767 V 08791 09176 1
2055	BCE		PC,WORK6,E	SHOULD BRANCH	12 08779 B 08792 09176 6
2056		H			1 08791 *
2057	* SUB-RTN 19.55		CHECK MLZW		
2058	PC	MLCWS	PERIOD,WORK6		12 08792 D 09067 09176 7
2059		MLZW	NWM04,WORK6		12 08804 D 09006 09176 F
2060	BW		*E13,WORK6	SHOULD NOT BRANCH	12 08816 V 08840 09176 1
2061	BCE		PD,WORK6,W		12 08828 B 08841 09176 #
2062		H			1 08840 *
2063	* SUB-RTN 19.56		CHECK MLCW		
2064	PD	MLCWS	DELTA,WORK6		12 08841 D 09077 09176 7
2065		MLCW	NWM16,WORK6		12 08853 D 09018 09176 G
2066	BW		*E13,WORK6,S	SHOULD NOT BRANCH	12 08865 V 08889 09176 1
2067	BCE		*E2,WORK6,B		12 08877 B 08890 09176 B
2068		H			1 08889 *
2069	WCP		PASS		10 08890 M 210 08921 W

CPU TEST
OPCODE OPERAND

CT ADDRS INSTRUCTION

PGLIN	LABEL	CPU TEST	CC01	PAGE
2070		BCB1 *-16	7 08900 R 08890	2
2071	BA1	*E1	7 08907 R 08914	G
2072		B QV	7 08914 J 08935	
2073	PASS	DCW @CC01 COMPLETE@.G	13 08921	
2074	CV	MRCWG RICE1.333		
2075		MLCS 332.339	12 08935 D 08967 00333	L
2076		B 322	12 08947 D 00332 00339	3
2077	RTC	BCB1 322	7 08959 J 00322	
2078		BA1 346	7 08966 R 00322 2	G
2079		B 1972	7 08973 R 00346	H
2080		DCW @Ma	7 08980 J 01972	
2081	*		1 08987	
2082	RESET	CW JF61	6 08988 H 03018	
2083		B START	7 08994 J 02000	
2084		H		
2085	*		1 09001 .	
2086	*			
2087	*			
2088	*			
2089	NWM00	DC a a		
2090	NWM01	a1a	1 09003	
2091	NWM02	a2a	1 09004	
2092	NWM03	a3a	1 09005	
2093	NWM04	a4a	1 09006	
2094	NWM05	a5a	1 09007	
2095	NWM06	a6a	1 09008	
2096	NWM07	a7a	1 09009	
2097	NWM08	a8a	1 09010	
2098	NWM09	a9a	1 09011	
2099	NWM10	a0a	1 09012	
2100	NWM11	a#a	1 09013	
2101	NWM12	a@a	1 09014	
2102	NWM13	a@a	1 09015	
2103	NWM14	aTa	1 09016	
2104	NWM15	aMa	1 09017	

DEFINE PRECEDING BRANCH LENGTH

CONSTANTS AND WORK AREAS

PGLIN	LABEL	CPU TEST OPCODE	OPERAND	CT	ADDRS	INSTRUCTION
2105	NWM16	S	aBa	1	09018	
2106	NWP17	a/a		1	09019	
2107	NWM18	aSa		1	09020	
2108	NWM19	aTa		1	09021	
2109	NWP20	aUa		1	09022	
2110	NWP21	aVa		1	09023	
2111	NWM22	aWa		1	09024	
2112	NWP23	aXa		1	09025	
2113	NWP24	aYa		1	09026	
2114	NWM25	aZa		1	09027	
2115	NWM27	a-a		1	09028	
2116	NWM28	a%a		1	09029	
2117	NWM29	a\$a		1	09030	
2118	NWP30	a@a		1	09031	
2119	NWM31	aMa		1	09032	
2120	NWP32	a-a		1	09033	
2121	NWM33	aJa		1	09034	
2122	NWM34	aKa		1	09035	
2123	NWM35	aLä		1	09036	
2124	NWM36	aMä		1	09037	
2125	NWM37	aNä		1	09038	
2126	NWM38	aOä		1	09039	
2127	NWP39	aPä		1	09040	
2128	NWM40	aQä		1	09041	
2129	NWM41	aRa		1	09042	
2130	NWM42	a-a		1	09043	
2131	NWM43	a\$ä		1	09044	
2132	NWM44	a@ä		1	09045	
2133	NWM45	aBa		1	09046	
2134	NWP46	a@ä		1	09047	
2135	NWM47	aLa		1	09048	
2136	NWP48	aEä		1	09049	
2137	NWM49	aAä		1	09050	
2138	NWM50	aBä		1	09051	
2139	NWM51	aCä		1	09052	
2140	NWM52	aDä		1	09053	

PGIN CPU TEST
OPCODE OPERAND

PGIN	LABEL	CC01	CPU TEST	CT	ADDRS
2141	NWP53	aEa		1	09054
2142	NWP54	aFa		1	09055
2143	NWP55	aGa		1	09056
2144	NWP56	aHa		1	09057
2145	NWP57	aIa		1	09058
2146	NWP58	aJa		1	09059
2147	NWP59	aKa		1	09060
2148	NWP60	aLa		1	09061
2149	NWP61	aMa		1	09062
2150	NWP62	aTa		1	09063
2151	NWP63	aWa		1	09064
2152	NWP64	aYa		1	09065
2153	*				
2154	TABLE	DCW	a/a	1	09066
2155	PERIOD		a/a	1	09067
2156	LOZNGE		aRa	1	09068
2157	RBRAKT		aJa	1	09069
2158	LESS		aTa	1	09070
2159	ALLBIT		aMa	1	09071
2160	AMPSND		aEc	1	09072
2161			aSa	1	09073
2162	SPLAT		aRa	1	09074
2163	RBRAKT		aBa	1	09075
2164			aJa	1	09076
2165	DELTA		aDa	1	09077
2166	CASH		a-a	1	09078
2167			a/a	1	09079
2168	COPMA		a/a	1	09080
2169	PERCNT		aRa	1	09081
2170	WDSEP	DC	aSa	1	09082
2171	BKSLSH	DCW	aSa	1	09083
2172	SEGMRK		aMa	1	09084
2173	SUBLNK		aBa	1	09085
2174	POUND		aRa	1	09086
2175	ATSIGN		aEc	1	09087

PG LIN	LABEL	CC01 OP COD	CPU TEST	CC01 OP REND	CT ADDRS	INSTRUCTION	PAGE 33
2176	CCLCN	•	a•a	a•a	1	09088	
2177	GREATR	aT•	aT•	aT•	1	09089	
2178	TPMARK	aMa	aMa	aMa	1	09090	
2179	QUESTN	aNa	aNa	aNa	1	09091	
2180	AYE	aAa	aAa	aAa	1	09092	
2181	EEE	aBa	aBa	aBa	1	09093	
2182	SEE	aCa	aCa	aCa	1	09094	
2183	CEE	aDa	aDa	aDa	1	09095	
2184	EEE	aEa	aEa	aEa	1	09096	
2185	EFF	aFa	aFa	aFa	1	09097	
2186	CEE	aGa	aGa	aGa	1	09098	
2187	ATTC+	aHa	aHa	aHa	1	09099	
2188	EYE	aIa	aIa	aIa	1	09100	
2189	EXCLAM	a•a	a•a	a•a	1	09101	
2190	JAY	aJa	aJa	aJa	1	09102	
2191		aKa	aKa	aKa	1	09103	
2192	ELL	aLa	aLa	aLa	1	09104	
2193	EMM	aMa	aMa	aMa	1	09105	
2194		aNa	aNa	aNa	1	09106	
2195	CH	aOa	aOa	aOa	1	09107	
2196	PEA	aPa	aPa	aPa	1	09108	
2197	QUEUE	aQa	aQa	aQa	1	09109	
2198	ARE	aRa	aRa	aRa	1	09110	
2199	RCDMRK	aTa	aTa	aTa	1	09111	
2200	ESS	aSa	aSa	aSa	1	09112	
2201	TEA	aTa	aTa	aTa	1	09113	
2202		aLa	aLa	aLa	1	09114	
2203	VEE	aVa	aVa	aVa	1	09115	
2204	CBLYCU	aWa	aWa	aWa	1	09116	
2205	EKS	aXa	aXa	aXa	1	09117	
2206	WYE	aYa	aYa	aYa	1	09118	
2207	ZEE	aZa	aZa	aZa	1	09119	
2208	NAUGHT	aOa	aOa	aOa	1	09120	
2209	CNE	aIa	aIa	aIa	1	09121	
2210	TWC	a2a	a2a	a2a	1	09122	
2211	THREE	a3a	a3a	a3a	1	09123	

CC01 CPU TEST
OPCODE OPERANDCC01
CT ADDRS
INSTRUCTION

PAGE 34

PGLIN	LABEL	CC01	CPU TEST	CT	ADDRS	INSTRUCTION
2212	FOUR		04a		1	09124
2213	FIVE		05a		1	09125
2214	SIX		06a		1	09126
2215	SEVEN		07a		1	09127
2216	EIGHT		08a		1	09128
2217	NINE		09a		1	09129
2218	*		T		1	09130
2219	K01	DC	aMa		1	09131
2220		DCW	aNa		2	09132
2221	K02		06ta		1	09134
2222	K03	DC	SSa		1	09135
		DCW	aBa		2	09136
2223			aNa		2	09139
2224	K04		D		1	09140
2225	K05		06ta		1	09141
			Ca		2	09143
2226	K06	DC	a a		1	09144
2227		DCW	at a		1	09145
2228	K07		aINA		2	09147
2229	K08	DC	06a		1	09148
2230		DCW	at a		1	09149
2231	K09		AMNa		2	09151
2232	K10	DC	0-6		1	09152
2233		DCW	at a		1	09153
2234	K11		aPNa		1	09154
2235	K12	DC	ay a		1	09155
2236		DCW	at a		2	09156
2237	K13	DC	Ca		10	09171
2238		DCW	aNa		4	09175
2239	K14		a ta		1	09176
2240	*					
2241	WORK1	DCW	a a		1	09158
2242	WORK2		a a		1	09159
2243	WORK3		a a		2	09161
2244	WORK4		a			
2245	WORK5		at S-a			
2246	WORK6		a a			

PGLIN	LABEL	CPU TEST	CC01	INSTRUCTION	
		OPCODE	OPERAND	CT	ADDRS
2282	BIGANS	a	GLL,D,R NTB,B,\$,RQPONMLKJ-a	33	09397
2283	MPYTBL	a	SEW,STG, AWSSZ,*ZYXWVUTS/BMT,3#0987654321 a	33	09398
2284				32	09462
2285				25	09487
2286		DCW	a-*0E6+0E-*0E-*0E-*0E+a	25	09512
2287		DC	a+CE-006-*EE-*00-*0E0*0E-6a	25	09537
2288	TRASH		a0E-*E-*00-*0E6*0E-*0E-*0E-a		
2289	*				
2290	LOADER	ECU	40C		
2291	TAD0	ECU	10C0		
2292	TAC1	ECU	10C1		
2293	TAD2	ECU	10C2		
2294	TAD3	ECU	10C3		
2295	TAD4	ECU	10C4		
2296	CPU	ECU	1256		
2297	MEMSIZ	ECU	1257		
2298	TYPE	ECU	18C0		
2299	1YPCK	ECU	1845		
2300	AA	ECU	1931		
2301	BLANK	ECU	TABLE		
2302	CBIT	ECU	NW#00		
2303	MINUS7	ECU	PEA		
2304	MINUS8	ECU	QUEUE		
2305	MINUS0	ECU	EXCLAM		
2306	DIVSCR	ECU	WORK7		
2307	CIVOND	ECU	WORK8		
2308	QUOREM	ECU	P1		
2309	QUOTNT	ECU	WORK10		
2310	XRO	ECU	24		
2311	TPMK	ECU	NW#15		
2312	CUQT	ECU	NW#31		
2313	DELT	ECU	NW#47		
2314	GPMK	ECU	NW#63		
2315	GMWM	ECU	ALLBIT		
2316	HOLDA1	ECU	HOLDA		
2317	HOLDA2	ECU	HOLDA		

CC01 PAGE 37
CT ADDRS INSTRUCTION

PGLIN	LABEL	CPU TEST OPCODE	OPERAND	CC01
2318	HOLDA3	ECU	HOLDA	
2319	HOLDA4	ECU	HOLDA	
2320	HOLD81	EQU	HOLDB	
2321	HOLD82	EQU	HOLDB	
2322	HOLD83	EQU	HOLCB	
2323	HOLD84	EQU	HOLCB	
2324	LTDORG *		09538	
		£54321		5 09542
2324		£9876		4 09546
2324		6123		3 09549
2324		£45679		5 09554
2324		-45679		5 09559
2324		-54321		5 09564
2324		-1		1 09565
2324		£9RIVIA		4 09569
2324		60		1 09570
2324		£7		1 09571
2324		£8		1 09572
2324		£1		1 09573
2324		J0		5 09578 03747
2324		JC		5 09583 03740
2324		RESET		5 09588 08988
2324		KFC2		5 09593 04504
2324		POUND		5 09598 09086
2324		KFC7		5 09603 04558
2324		KF06		5 09608 04551
2324		£00101A		5 09613
2324		£00102A		5 09618
2325	END	2000		J02000

END OF ASSEMBLY

